DESIGN OF X-Y PLOTTER

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

BY
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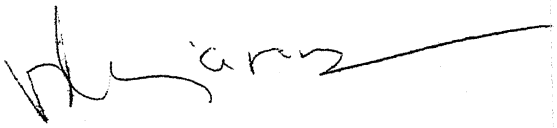
to the

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY KANPUR
AUGUST 1971

CONTENTS

CERTIFICATE

This is to certify that the work entitled, "X-Y PLOTTER" for this thesis has been carried out under my supervision and this work has not been submitted elsewhere for a degree.



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August 1971

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- K. Venkatachalam

August 1971

ABSTRACT

In many analog simulation experiments X-Y plotters are used as output devices. Servomechanical recorders have good accuracy, but have poor frequency response and also they are expensive. A X-Y plotter without servo-motors and using mainly electronic circuits has been designed and fabricated. In this plotter mostly indegeneous components are used.

The principle of "plotting a curve using a finite number of points" has been used. Analog signal to be plotted is converted into digital form, which is used to select points from an (8x8) matrix of points. Selection is done by coincidence technique (coincidence of X and Y wires). Instead of using one pen and moving it to each point for plotting, a small felt pen is kept at each point. These pens will make marks on the paper kept above, whenever they are selected. This eliminates X and Y direction movements of the pen increasing the frequency response of the plotter. Suggestions have been made to improve this model.

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CHAPTER 1

INTRODUCTION

Every electrical signal which carries information is a function of time. It is necessary in a number of applications to have accurate record of the signal. In many analog simulation experiments it is necessary to plot a graph of two related variables X(t) and Y(t) - one against another.

This can be done using cathode ray oscilloscope and photographing it, or using an electromechanical recorder. Cathode ray oscilloscopes have higher bandwidth, but photography is expensive. Servomechanical recorders have good accuracy (1%) but have poor frequency response, the bandwidth being 0-100 Hzs due to the physical movements involved. Further servo motors are expensive.

Hence the aim of this project is to design a X-Y plotter for analog computer satisfying the following conditions.

1. The bandwidth of the plotter should be 0-1 KHz so that it can be used for recording the output of the analog computer without recorder limitation in time scaling.

2. The plotter should be built as far as possible using indegenous components.

3. The design should be flexible so that both discrete and integrated circuit components can be used to minimise the cost.

4. The plotter should be rugged such that it can be used by the students in the regular laboratory experiments.

5. The total cost of the plotter should not exceed 1000 rupees.

Servo-mechanical plotter

The electromechanical X-Y recorders usually record two analog input variables simultaneously, employing two identical, independent, self balancing, closed loop servomechanisms. One controls the motion in X direction and other in Y direction proportional to the input signals representing the two related functions. The pen, by its position on the arm, generates a position voltage at all times, indicating the actual position of the pen with respect to the zero point. External input voltage is subtracted from this voltage and the difference voltage, after being converted into a suitable form (modulated a.c. signal), actuates the control winding of a 2-phase induction servomotor. When the pen reaches the desired

position the actuating signal becomes zero.

The main factors limiting the frequency response of this type of plotter, are the speed response of servo-motors, and mechanical arrangements for the movement of the pen. Further, these motors are expensive. Hence the idea of using servomotor was rejected. So it is necessary to try the feasibility of some other plotting mechanism which does not require sluggish servomotors.

Plotting by points

Any curve can be represented using a finite number of points. The number of points needed depends upon the accuracy needed and rate of change of slope of the curve. So it is sufficient if we plot a curve using a finite number of points. This type of plotting makes it feasible to use digital circuits instead of analog circuits. Digital circuits are less expensive due to their modular structure. The cost of analog circuit increases exponentially with accuracy desired whereas the cost of digital circuit increases only linearly with accuracy.

Thus it was decided to design a plotter which will sample and quantize the curve and plot individual points of the curve. An (8x8) matrix of points is chosen for plotting. It is assumed that the analog signal Y(t) varies between $\pm$ 3.5 volts and X(t) varies between 0 and

8.5 volts. Therefore 8 voltage levels at a one volt step, along both the axes cover the entire plotting range. The quantization can be pictured as a set of parallel wires denoting discrete voltage levels, covering the entire plotting range. Two such sets are placed mutually perpendicular to each other and the points of intersection of these lines form (8x8) matrix of points.

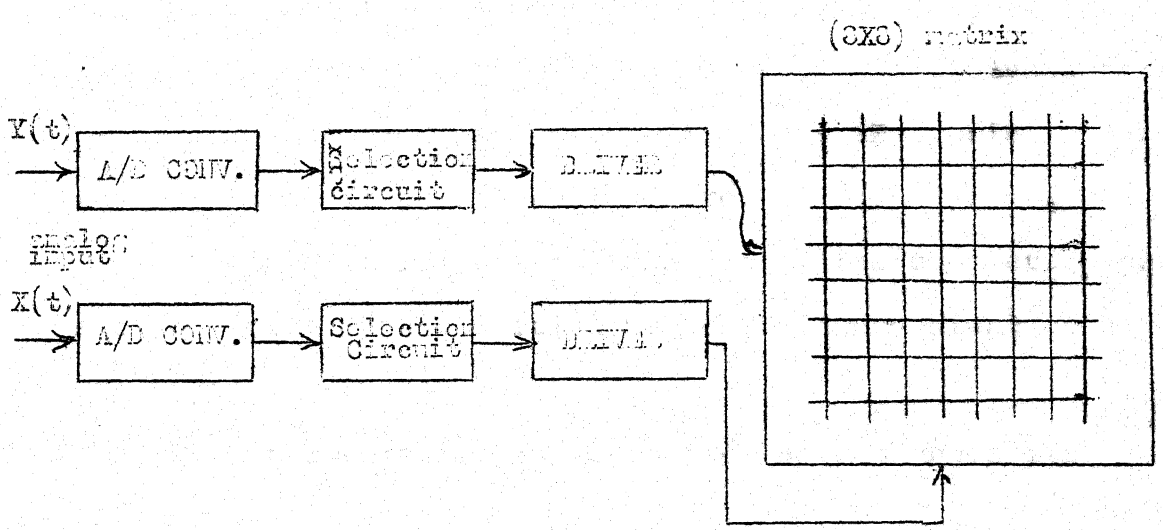


Figure 1: Block diagram of the proposed plotter

In Figure 1 block diagram of the proposed plotter is given. The analog signal to be plotted is converted into digital form in each sampling interval by the analog to digital converter. The digitised values of X(t) and Y(t) are used to select any one of the points in each interval by coincidence technique. When a particular point is selected, a mark is to be made at that point.

Different techniques of plotting points were tried[1]. They are described below.

Method 1

A potential difference is created between two sides of a paper soaked in some electrolyte like $K_2Cr_2O_7$ or KI or $CuSo_4$, at the selected point. Due to electrolysis taking place some coloured mark is developed at that point. But the drawbacks of this technique are:

1. For electrolysis to take place, the complete paper must be wet. This condition makes it inconvenient to handle the paper.

2. After sometime the complete paper changes its colour.

Method 2 - Light sensitive paper

At each plotting point a small bulb is kept. Whenever a particular point is selected, the bulb at that point lights. Over the bulbs some transflucent sheet

is kept and small holes, one corresponding to each bulb are made. An ammonia paper on which the point is to be taken, is placed with the sensitive side facing the bulbs. When a bulb lights, a fine beam of light passes through the hole, producing a mark on the paper. Since it takes about 5 minutes to record a mark, this method is too slow for the present application.

Method 3 - Teledeltax paper

When a potential difference of 5 to 10 volts is established between the two sides of Teledeltax paper, a spark is produced which makes a hole at that point. But this paper is expensive and hence cannot be employed for regular use.

Method 4 - Heat sensitive paper

The selected points can be marked by using heating elements in the plotter. Whenever a particular heating element is selected, current is passed through it and it gets heated up. This is made to make a mark on the heat sensitive paper (Sanborn's Paper) kept above. But the time required to get sufficient heat is of the order of 1 sec and the paper is expensive.

Method 5 - Use of ordinary paper and felt pens

Marks can also be made by keeping small felt pens at each point. Whenever a particular point is selected the

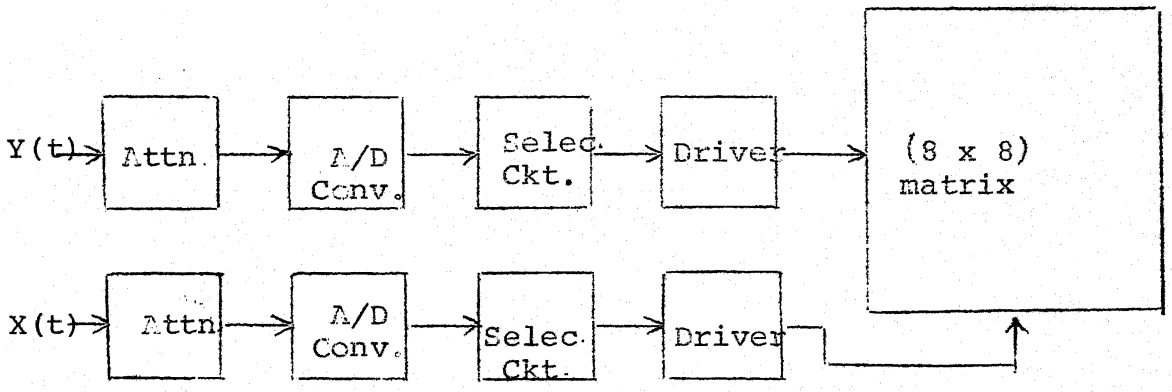
corresponding pen is lifted up which makes a mark on the paper kept above. The lifting of the pen can be achieved by using small permanent magnet and a moving coil enclosing the magnet. Whenever a particular point is selected current is passed through the coil. The coil moves up due to the force of repulsion and hence the pen is lifted up. To get appreciable movement, the current through the coil should be maintained atleast for 20 msec. This will again affect the bandwidth of the plotter. To overcome this some electronic circuits are used.

In the following chapters the design of a plotter using felt pens is discussed in detail.

CHAPTER 2

SYSTEM DESIGN

2.1 Specifications



Attenuator: The output from the analog computer (input to the plotter) varies between -10 volts and + 10 volts. The signal is attenuated such that it varies between -3.5 Volts and + 3.5 volts. One 10 K ohm potentiometer is used as attenuator.

Analog to Digital Convertor

Simultaneous conversion technique is used here. The maximum conversion rate of A-D convertor should be 8 KHzs. A detailed discussion of some other familiar techniques is

given in Appendix A which will be helpful when one would like to improve the accuracy of this plotter.

The selection circuit selects any one of the 8 wires during each interval depending upon the digital output of the analog to digital convertor. The driver feeds 50 ma current to the coil at the selected point. The mechanical construction of (8x8) matrix of points is given in Appendix B.

2.2 Analog to Digital Convertor

A voltage analog to digital convertor can be defined as "a device that accepts a voltage parameter as input and produces a coded digital signal as its output". Different techniques of analog to digital conversion are available. Here simultaneous conversion technique is used because it is cheaper when the number of bits used (3 bits in our case) is small. It is also faster.

Simultaneous Conversion Technique

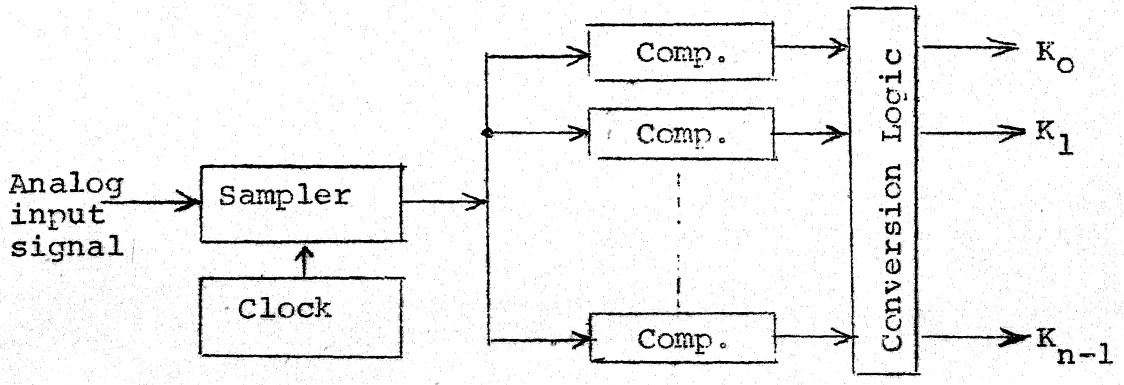


Figure 2: Simultaneous Conversion Technique

The input analog signal is sampled at a rate determined by the clock frequency. The output of the sampler is fed simultaneously to 8 comparators each of which responds to a different level of input voltage. Each comparator determines only one unique quantization level. The output of the comparators are fed to the conversion logic which gives the digital output. This digital value corresponds to the sampled analog input at that interval of time.

CHAPTER 3

DESIGN OF INDIVIDUAL BLOCKS

3.1 Clock

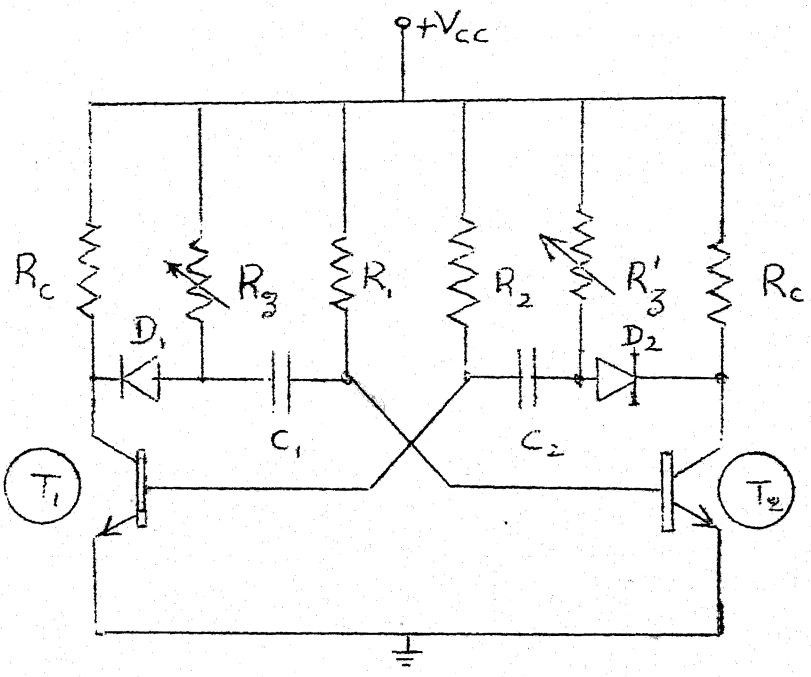


Figure 3: Clock

This particular configuration of astable is used to get good collector waveform with vertical edges. In the conventional type of astable the leading edges will not rise sharply due to the base current of the transistor in saturation, flowing through the collector load of the transistor in cut off. When T_1 is driven off, its collector goes to $+V_{cc}$ and so D_1 is reverse biased and T_2 goes into saturation.

The saturation base current of T_2 passes through C_2 and R_2 and not through R_{c1}. Since I_B' no longer passes through R_c the collector waveform has vertical edges. In Figure 3, R_3 and R_3' are two ten turns helical potentiometers. By varying this we can get linear variation of the frequency of oscillation. The clock is designed such that the frequency can be varied continuously from 10 Hzs to 800 Hzs in two steps.

3.2 Sampling gate

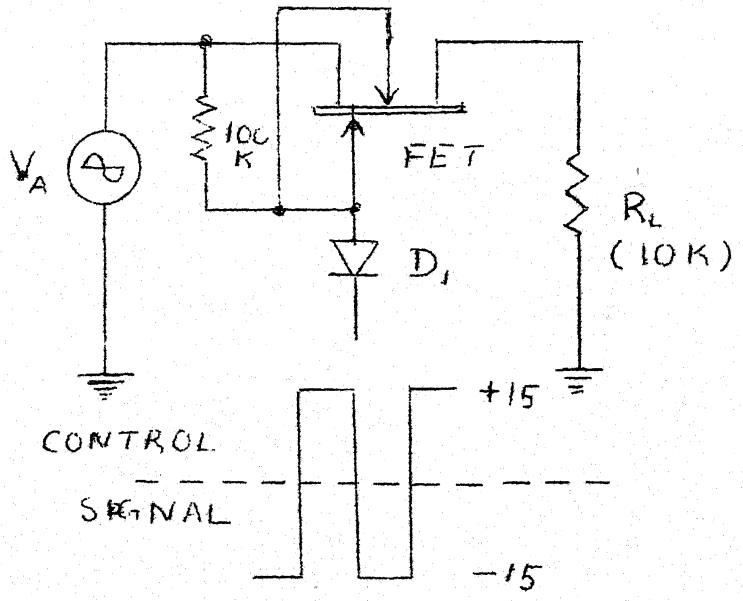


Figure 4: Sampling Gate

A single FET is used as series chopper. The output from the clock after proper level shifting (±15V) is used as control signal for the sampling gate. The control signal is applied to the floating end of the diode D, in Figure 4. When the control signal is positive (+15V) the

diode D_1 is reverse biased. The 100K resistor from source to gate will make the gate follow the input potential as long as D_1 is reverse biased. Hence the input analog voltage appears across R_L. When the control signal is negative (-15V) the diode D_1 starts conducting and hence negative potential appears between gate to source and the FET turns OFF. Thus we get, at the output, the sampled input analog signal.

3.3 Comparator

Schmitt Triggers with different reference voltages (each corresponds to one quantization level) are used as amplitude comparators.

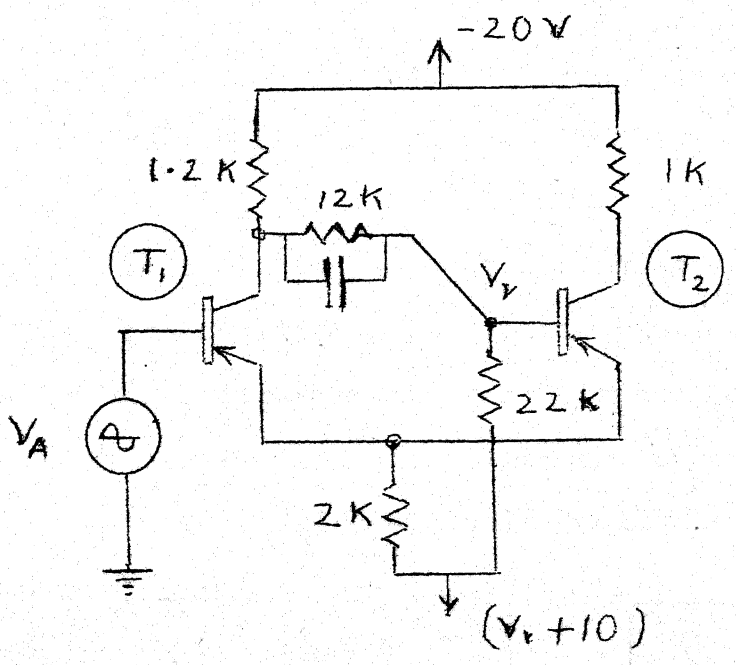


Figure 5: Schmitt Trigger

V_r corresponds to one of the quantized voltage levels. Both V_r and (V_r+10) are applied externally. The transistor T_2 is normally off giving -20V as output. Transistor T_1 will remain conducting and the corresponding collector voltage being -15V. All comparators get the sampled voltage from the gate through a buffer. Whenever the sampled voltage is greater than V_r, then all such comparators will change their states bringing T_1 to cut off and T_2 to conducting. The corresponding output voltage of T_2 is -15V. Now we have to find that comparator with highest reference voltage and which has also changed its state (T_2 conducting). The reference voltage corresponding to this comparator is the quantized value of the sampled analog voltage. The selection of the comparator with highest reference voltage is done by "selection circuit" which will be discussed in the next section.

Before that let us see what are the special merits of this particular Schmitt trigger configuration. Normally in other Schmitts where external threshold is not applied there will be some hysterisis which is due to the upper and lower trip points occuring at different voltage levels as shown in Figure 6.

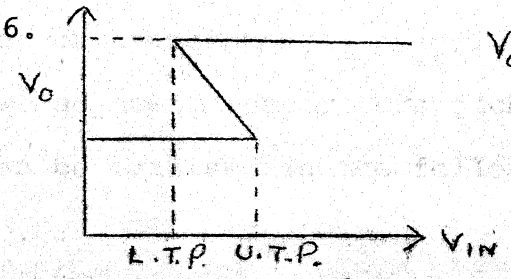


FIGURE-6

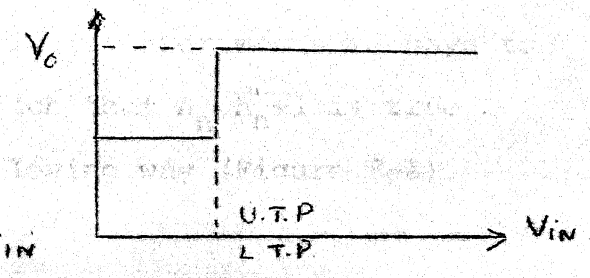


FIGURE-7

Since in our circuit we use external voltage as reference voltage, both U.T.P. (upper trip point) and L.T.P. (lower trip point) lie in the same voltage level as shown in Figure 7. The other advantage is that in this Schmitt trigger, irrespective of the threshold voltage, the ON voltage is -15 volts and OFF voltage is -20 volts whereas in the normal configuration, where there is no externally applied reference voltage, the ON output voltage will be different for different upper tripping points. Thus this particular configuration used is very convenient for performing logical operations. To get the various reference voltages, potential dividers [1] are used.

3.4 Selection Circuit

As we have seen before we have to select that Schmitt trigger with highest reference voltage and which has also changed its state. Suppose we represent the two states of the comparator as A_n and $\bar{A}_n$ where A_n denotes (-15V) and $\bar{A}_n$ denotes -20V. Now our problem is to find two adjacent comparators, one comparator being in -15V state and the next one being in -20V state (Here -15V and -20V are corresponding to the collector voltages of transistor T_2 only). In other words we have to find two adjacent comparators such that $A_n.\overline{A_{n+1}}$ is true. This can be realised in the following way (Figure 8-a).

But the above direct realisation using separate gates needs two logical gates for each set of comparators. The same logical function can be realised using one n-p-n transistor as shown in Figure 8-b.

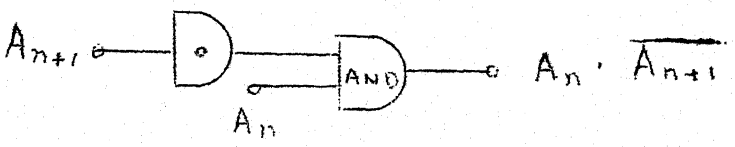


Figure 8-a.

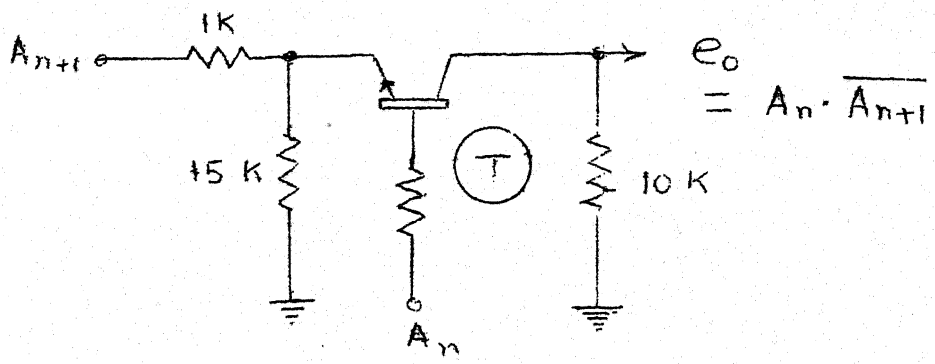


Figure 8-b: Selection circuit

e_o can be calculated when A_n = -20 volts and A_{n+1} = -20 volts as given below:

$$V_E = -20 \times 15/16 = -17.6V \qquad V_B = -20V$$

Since the emitter base junction is reverse biased, the transistor is in the cut off and hence $e_o = 0$.

Let A_{n+1} = -20 volts and A_n = -15 volts.

Now V_E = -17.5 volts V_B = -15 volts

Here emitter base junction is forward biased and hence V_E appears in the output. Similarly it can be seen that when

A_{n+1} = -15 volts and A_n = -15 volts the transistor is in cut off mode.

Thus it is seen that the above circuit always selects the adjacent pair comparators that hold complementary outputs.

The output of selection circuit is either -17.5 V or 0 volts. The difference in voltage levels is very high. It will be convenient if the logical levels are made as +3.5 volts and 0 volt. This can be achieved by using the following circuit (Figure 9) which shifts the levels correspondingly.

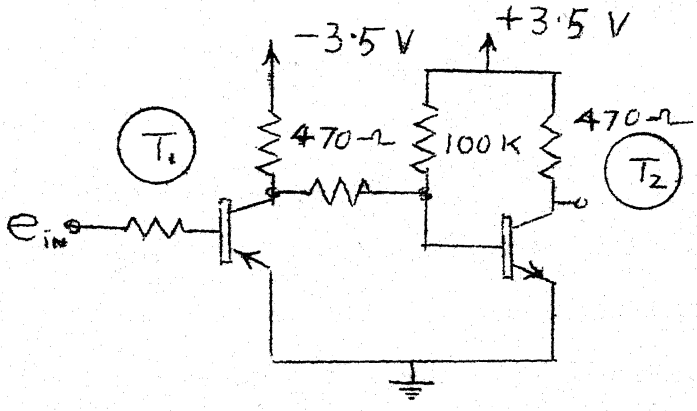
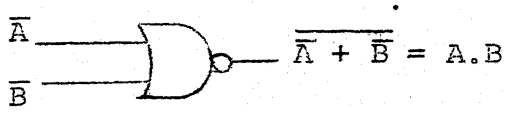


Figure 9: Logical level shifter

When e_{in} is 0 volt e_o is + 3.5 volts and when e_{in} is -17.5 volts e_o is 0 volt (Figure 9). It can be seen that logic levels are shifted to 0 volt and +3.5 volts and also the logical variable appear in the complemented form. This will be useful latter when AND function is obtained using NOR gate (MC 824)



3.5 Pen Driver

As explained before, felt pens with magnets and moving coils are used for plotting. The magnet used is cylinderical permanent magnet of size 7mmx12mm. The arrangement of the magnet is given in the Figure 10.

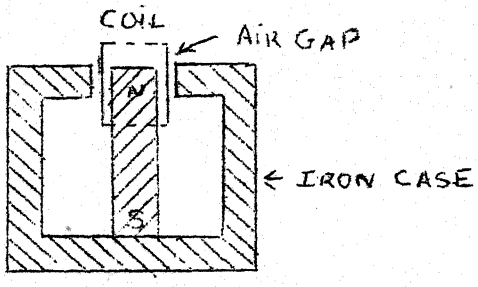


Figure 10: Magnet and Coil

In the air gap the field is radial. A small coil is kept in the air gap so that it encloses the magnet and can also freely move up and down. Whenever 50 ma of current is passed through the coil, the coil moves up or down depending upon the direction of the current. The force with which the coil moves up is sufficient to lift the small felt pen.

But it is observed that unless the current through the coil is maintained for atleast 20 msec, we could not get appreciable movement of the coil. Hence for plotting each point we have to spend atleast 20 msecs. To plot a full waveform, if we use 8 points, then the total time taken for plotting one full cycle is 160 msec. Hence the bandwidth

of the plotter is only 6 Hzs. This is poorer than mechanical plotter.

So in order to increase the badwidth, which is one of the motivations of this project, we should either try to decrease this 20 msec time or find some means which overcomes this. The circuit shown in Figure 11, is used which will effectively serve our purpose.

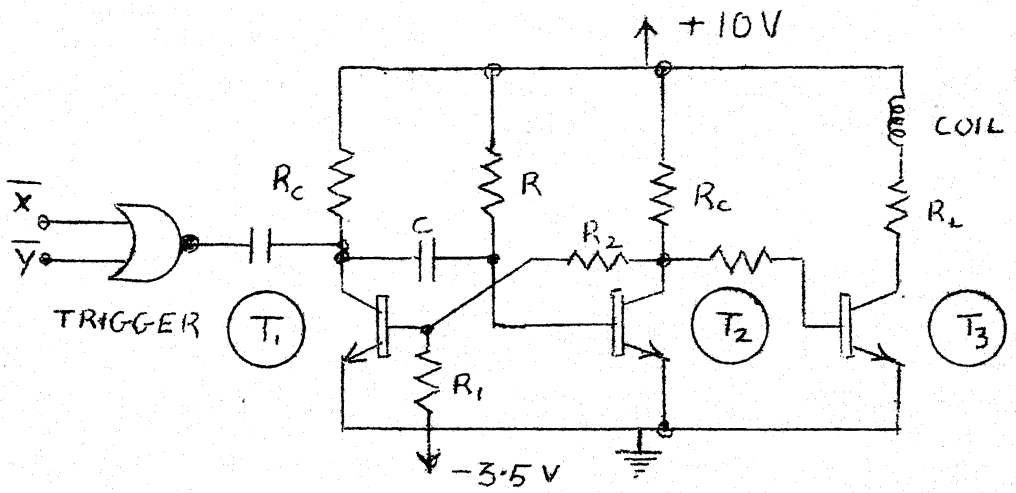


Figure 11: Driver

Transistors T_1 and T_2 form one-shot multivilerator with a time delay of 40 msec. T_2 is normally in saturation and T_1 in cut off. The base of T_3 is returned to collector of T_2 through a 1.2K resistor. Hence whenever T_2 is in saturation, T_3 is cut off and whenver T_2 is cut off T_3 conducts. The moving coil and a series resistance, form the collector load of the transistor T_3. Whenever a particular point is to be selected we pulse the corresponding monostable multivilerator, so that T_2 cuts off and T_3 conducts.

Since the delay is adjusted for 40 msec T_3 will remain in conduction for 40 msecs. Hence the coil in the collector will be getting enough current continuously for 40 msecs.

Here one important thing to be observed is that the minimum pulse width required to trigger the multivibrator is only of the order of 50 n secs. So once we pulse the monostable multivibrator, we need not wait until the coil moves up and we can proceed to select the next point. In other words we can sample the input analog voltage as fast as 10^6 samples per sec. So the mechanical time constant of the moving coil no more restricts the bandwidth of the plotter.

Another technique that could have been used is to have core memory. The input signal is digitised at high rate and stored in the memory. Then the memory can be scanned at a lower speed as required by the moving coil. Of course this needs extra scanning and control circuits, thus increasing the cost.

CHAPTER 4

CONCLUSION

In this method the distance between two points cannot be reduced by less than 7 mm. This is due to the restriction imposed by the physical dimensions of the magnets used. Besides this the ink in the pens used for the plotting if exposed for a long time to the atmosphere dries up. However, arrangements have been made to shield all the pens when the plotter is not in use.

To eliminate the above problems, heating elements are used in place of pens and the experiment turns out to be practical. Heater elements are fixed on small bases and they are kept heated permanently. Whenever a particular point is to be selected, the coil lifts the heater base and hence mark is made on the Sanborn's paper kept above. The method is found satisfactory and if desired all the pens may be replaced by heater elements.

Performance of the plotter

The plotter is built using mostly indegeneous components except for a few I.C. gates. The cost of the plotter having (8x8) matrix points is within 1000 rupees. However, to get a good plot one should have (20x20) matrix points. But this will increase the cost.

Drawbacks

1. Felt pens are inconvenient because they need periodic inking.
2. Due to the physical dimensions of the magnet, the resolution becomes poor. The distance between two points can not be reduced by less than 7 mm.

Suggestions for future work

The plotter may be improved by making the following modifications. Instead of felt pens small heater elements which can be heated sufficiently with a current of 100 milliamps and within a time of 100 millisec, are to be used. In this case we need not use the permanent magnets and the moving coil. Hence the cost is reduced and the resolution can also be improved by having two points as near as 3 mm or even less. In this case the heater elements form the loads of transistors T_3 in Figure 11. The heat sensitive paper will be kept pressed against these heater elements. For a good plotter, one should have atleast (20x20) matrix points, which can be obtained without any mechanical difficulties.

We can easily get low time constant heater elements by using the following technique. The thermal time constant for a given structure depends upon its thermal mass, which

includes the physical size of the heated material and the thermodynamic mechanism acting to conduct energy away from it. So thin film resistors can be used as heating elements which will have low thermal rise time constant. The choice of substrate over which the film is made largely governs the fall time. Hence for higher speed consideration one has to choose the suitable combinations of resistor element and substrate. Thin film silicon resistor and ceramic substrate (Al_2O_3) are proved to be a good combination. This type of plotting head will require only 10 msec current pulse corresponding to a power level of 100 mw/point to achieve 200°C peak temperature. The life of the plotting head is also found to be high ($50x10^6$ points).

Here thin film resistors can be heated in 100 millisec with a current less than 100 m.a. and the points can be as near as 2 mm. By changing the monostable time delay (100msec) and the collector load resistance of T_3 in Figure 11 (to get sufficient current), the same hardware can be used for the plotter, using thin film heater elements.

REFERENCES

1."X-Y Recorder With No Moving Parts", Shri Dhar and Shrawan K. Agarwal, Undergraduate Project, Electrical Engineering Department, Indian Institute of Technology, Kanpur, 1967.

2."Application Notes on Analog to Digital Conversion Techniques", Motorola.

3."Semiconductor Data Handbook", Motorola

4."A New Printing Principle", W.H. Puterbaugh and S.P. Emmons, Spring Joint Computer Conference, Vol. 30, 1967, pp 121.

5."Pulse, Digital and Switching Waveform", Jacob Millman and Herbert Taub.

6."Transistor Electronics", Clarkes and Joyce, McGraw-Hill.

7."Transistor Circuit Design", Texas Instruments.

APPENDIX A

ANALOG TO DIGITAL CONVERSION TECHNIQUES

A voltage analog to digital converter can be defined as "a device that accepts a voltage parameter as input and produces a coded digital signal as its output".

A-D conversion can be divided into two basic groups:

1. Open loop type
2. Feedback type

The openloop converter generates a digital code directly upon application of an input voltage, which is generally asynchronous. Whereas in feedback technique a series of digital numbers is generated, reconverted into analog voltage and compared to the input analog voltage. This goes on until both the analog voltages are very nearly equal and the corresponding digital output is the digitised value of the signal.

There are different techniques available under each group.

Open loop technique

1. Analog to frequency
2. Analog to pulse width
3. Simultaneous conversion

Feedback technique

1. Ramp and counter methods
2. Successive approximation
3. Sub ranging method
4. Double ramp

Open Loop Technique

Analog to frequency

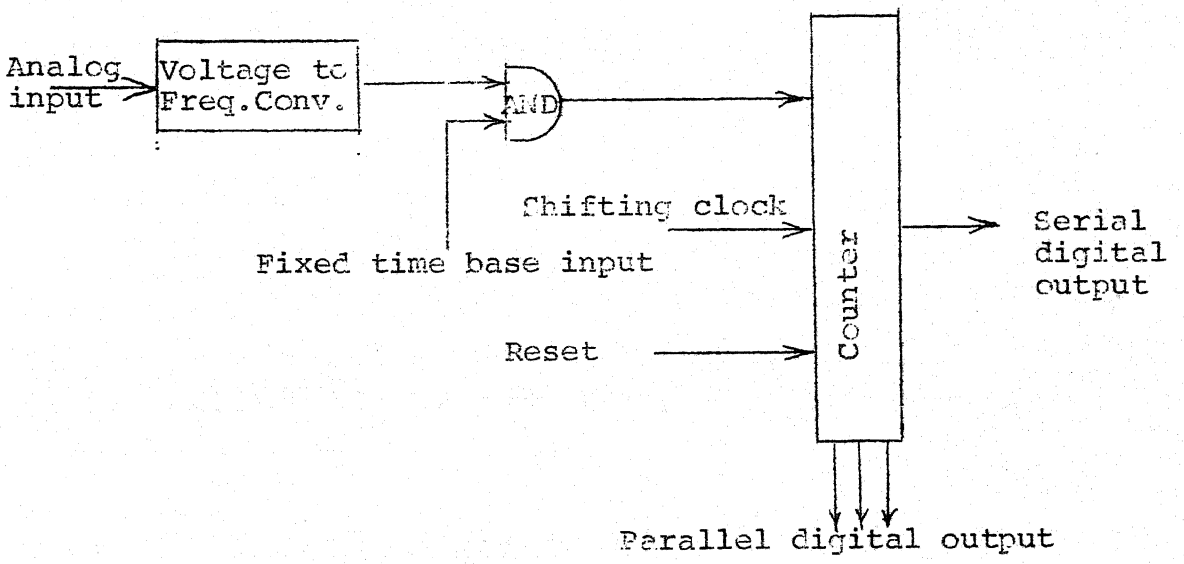


Figure 12: Analog to frequency conversion

This is the most popular one due to its simplicity. The voltage to frequency converter produces a signal whose frequency will be a linear function of analog input voltage. Voltage controlled oscillator (V.C.O) is a circuit of this type. The "fixed time base signal" is a digital pulse whose ON period is known and very precise. An accurate delay circuit will produce a pulse of this type. The leading edge of this fixed time base signal will gate the output of the oscillator (properly shaped) to the counter. The counter is initially at reset. The oscillator output after proper shaping is applied to the counter for the given interval of the time, i.e. ON period of the fixed time base signal. The reading

shown by the counter after ON period is the digital representation of the analog input voltage. Accuracy limitation in this technique is due to the non-linearity of the V.C.O.

Analog to pulse width converter

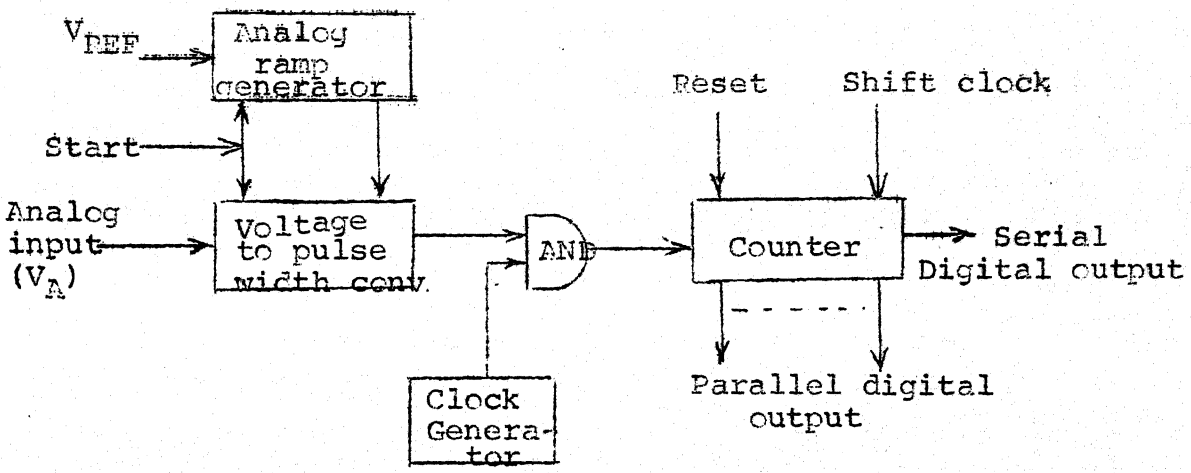


Figure 13: Analog to pulse width conversion

Here a pulse whose width is proportional to the input analog voltage is generated. This pulse controls the input to the counter from the fixed frequency clock generator. Thus the number of clock pulses to the counter is proportional to the pulse width which in turn is proportional to the input analog voltage. At the end of this operation, the reading given by the counter is the digitised signal. Suppose at the end of the pulse the counter is in state N, a fraction

of its maximum value, and the binary fraction N accumulated in the counter satisfies the equation

$$V_A = N\ V_{ref}$$

where V_A is unknown analog voltage and V_{ref} is the reference voltage or maximum ramp voltage.

Feedback Technique

In this type of analog to digital converters, comparator is used which compares unknown analog voltage with some standard reference voltage V_D and indicates which is greater and this result is used for further control operation, which will in turn either increase or decrease V_D by one step. The process is repeated until V_D and V_A are very nearly equal. Generally V_D is generated by using ladder network (digital to analog conversion).

Continuous counter encoder

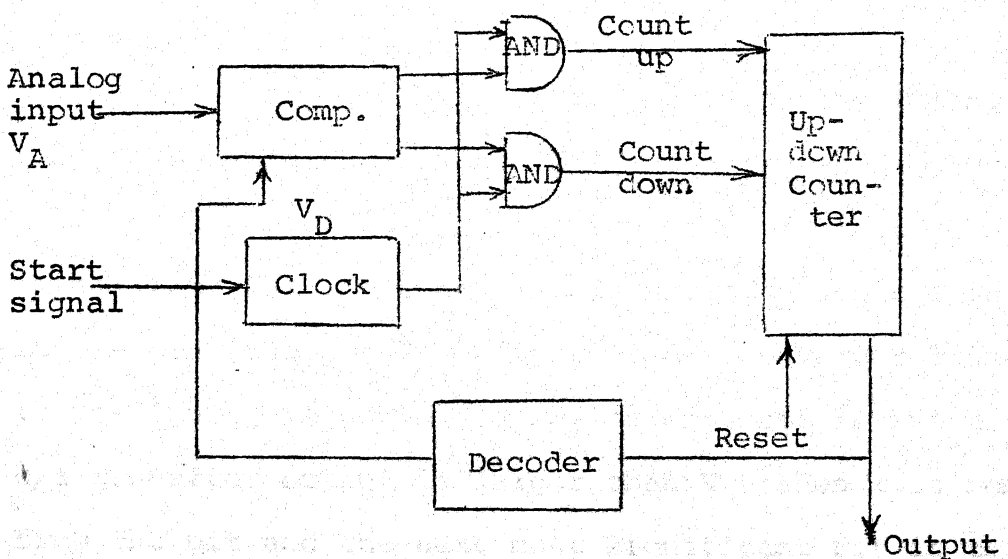


Figure 14: Continuous counter encoder

Input analog signal is compared with the reference signal from the output of the decoder. If $V_A > V_D$ then count up operation will be activiated. If $V_A < V_D$ then count down operation will be done. The process is carried over until V_A is differing from V_D by less than one step voltage and the corresponding counter reading will be digital output.

Successive approximation technique

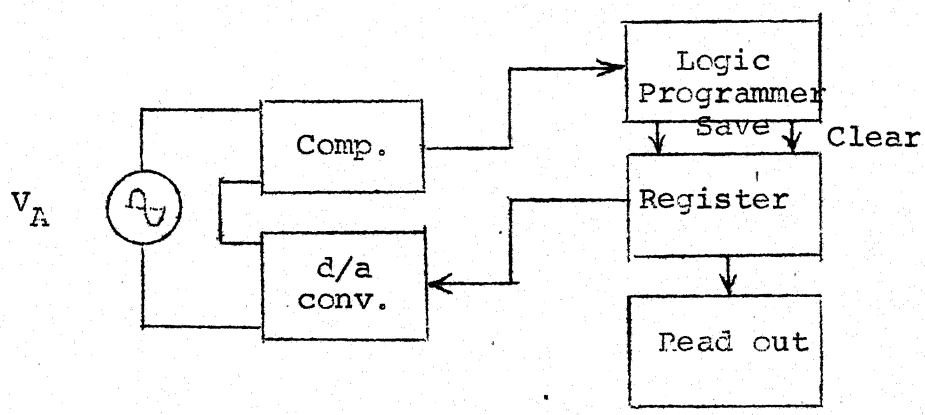
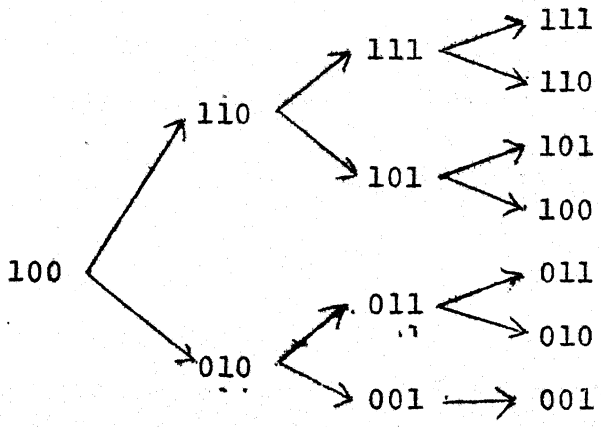


Figure 15: Successive approximation technique

This technique is one of the fastest and most commonly used. The conversion process consists of starting with the most significant bit and successively trying a logic 1 in each bit of d/a conversion. The output of d/a converter is compared to the analog input voltage V_A as each bit is tried. If d/a converter output is larger than V_A, then 1 is removed from the bit and the next most significant bit is tried. When

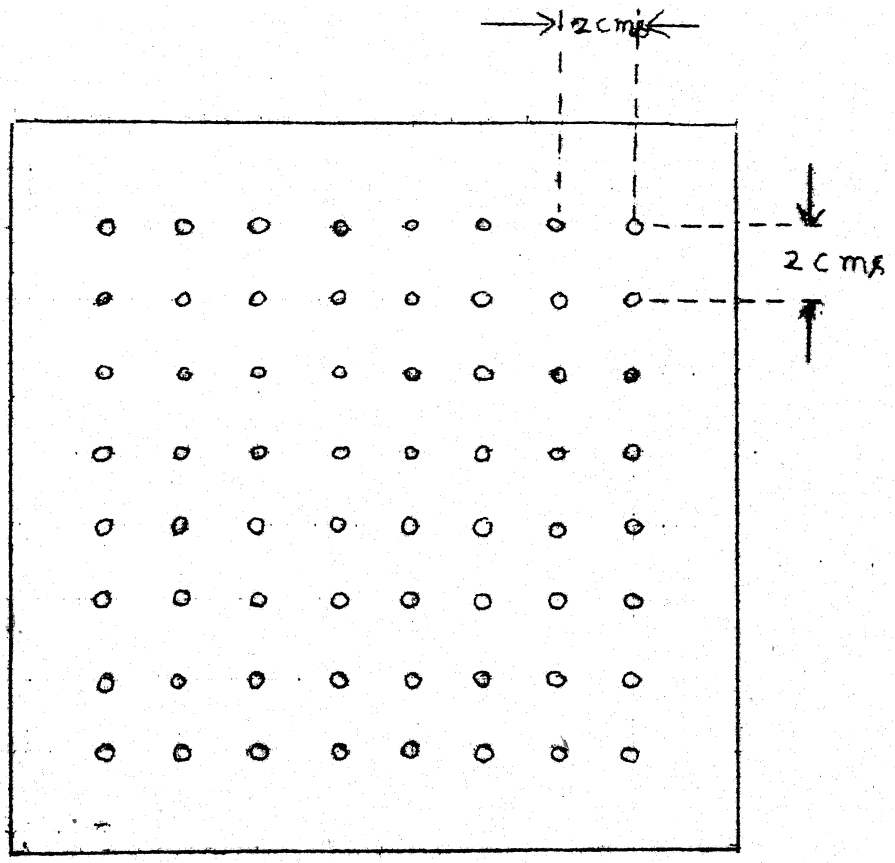
V_A is larger, then 1 remains in the bit. After the least significant bit is tried, the digital word in d/a converter is equivalent to the analog input voltage.

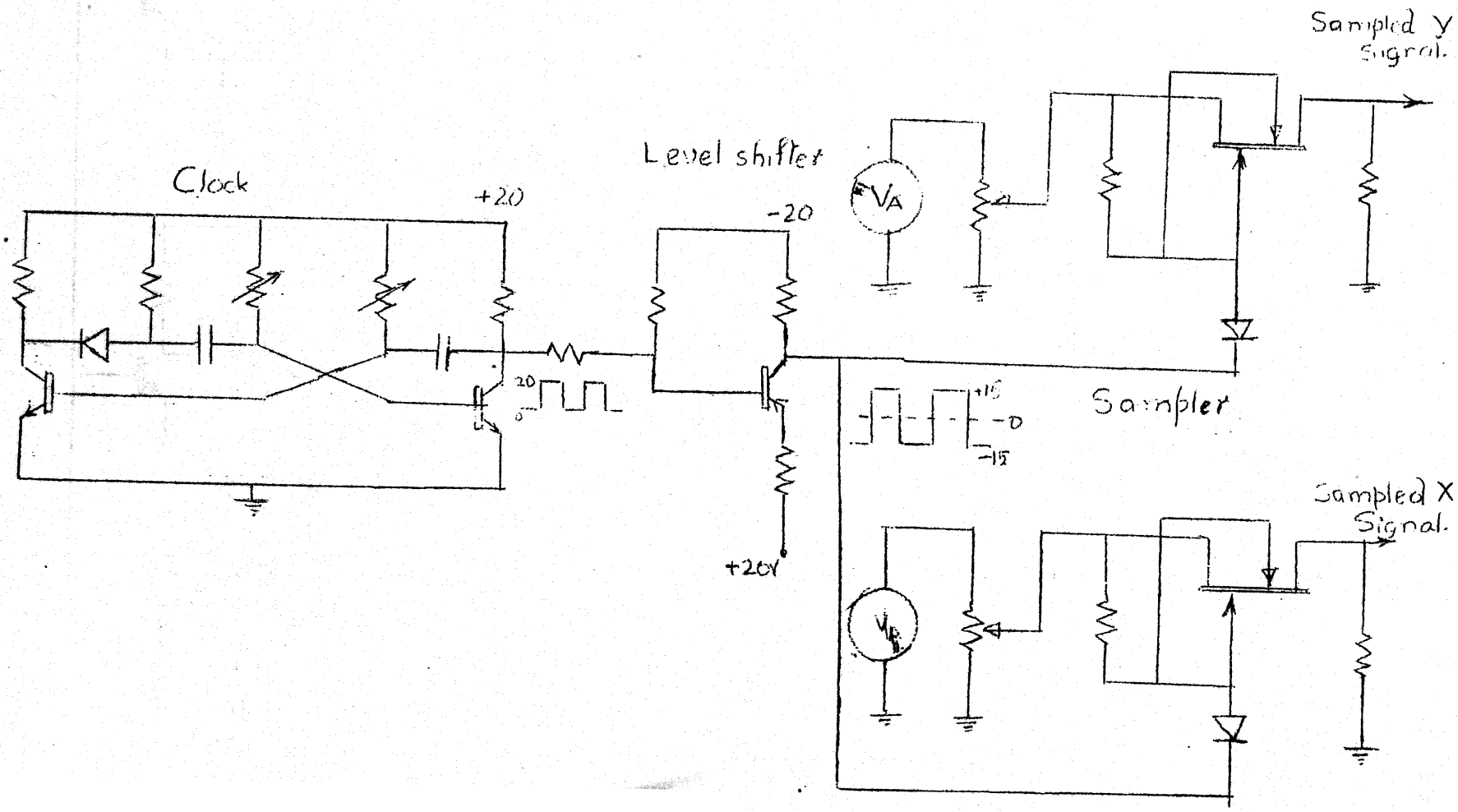
Illustration of 3-bit successive approximation conversion technique is given below.

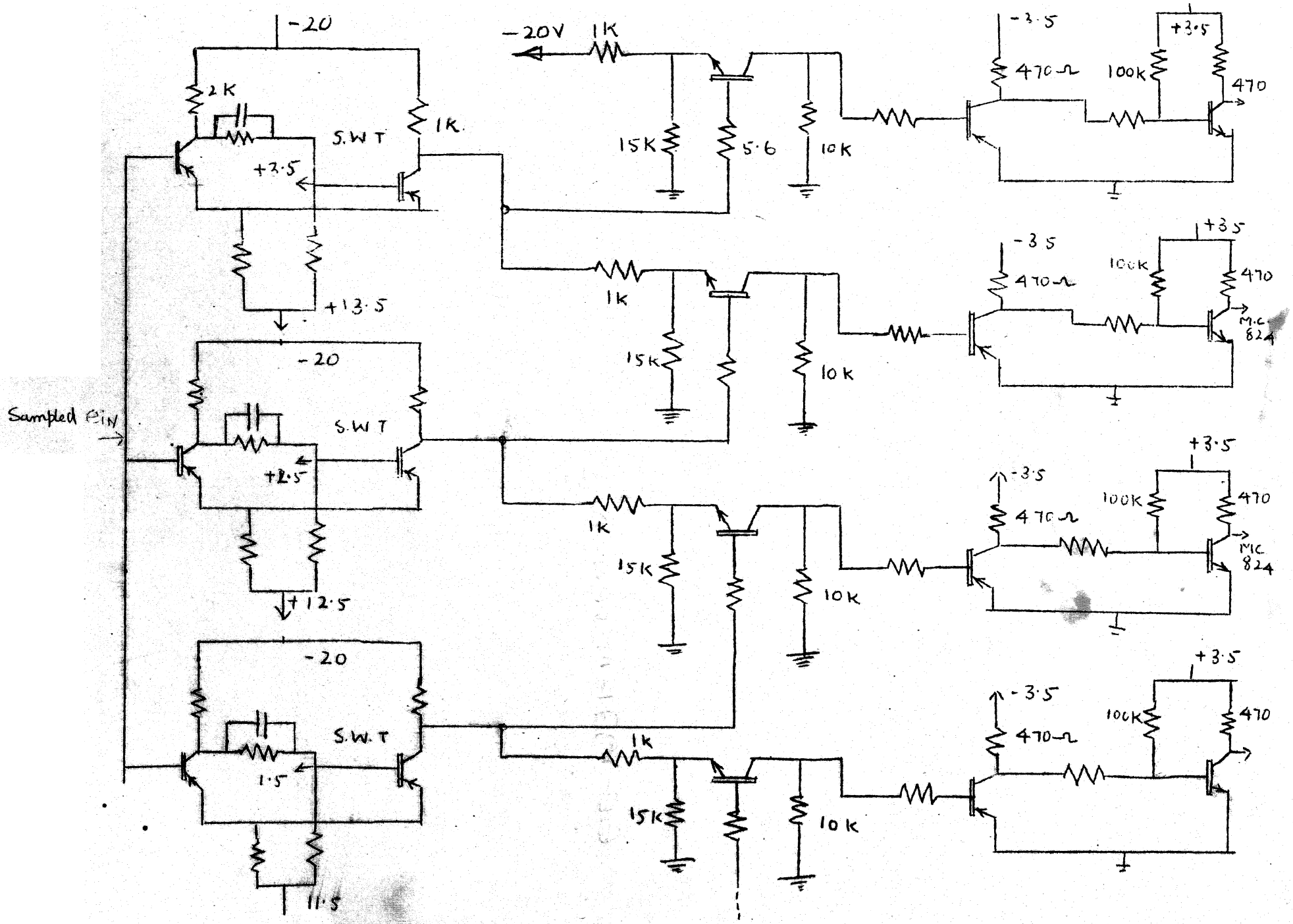


APPENDIX B

LAYOUT OF (8 x 8) MATRIX




Sampled Y Signal.
Level shifter
Clock
+20
-20
V_A
20
0
+15
-0
-15
Sampler
+20V
Sampled X Signal.


-20
2K
S.W.T
1K
+3.5
+13.5
-20
S.W.T
+2.5
+12.5
-20
S.W.T
1.5
11.5
Sampled e_{IN}
-20V
1K
15K
5.6
10K
1k
15K
10k
1K
15K
10K
1k
15K
10k
-3.5
470
100K
+3.5
470
-3.5
470
100K
+3.5
470
MIC 824
-3.5
470
100K
+3.5
470
MIC 824
-3.5
470
100K
+3.5
470

EE-1971-M-VEN-DES